

AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please add new claims 21-23.

1. (CURRENTLY AMENDED) A prescaler comprising:

a first circuit configured to present generate a plurality of control signals in response to a first clock signal having a first frequency;

5 a multiplexer configured to multiplex a plurality of data signals in response to said control signals to present a second clock signal having a second frequency that is a non-integer fraction of said first frequency; and

10 a second circuit configured to present (i) generate said data signals in response to said second clock signal and (ii) present said data signals directly to said multiplexer.

2. (ORIGINAL) The prescaler according to claim 1, wherein said second circuit is further configured to sequence said data signals through a plurality of patterns response to said second clock signal.

3. (ORIGINAL) The prescaler according to claim 1, wherein said second circuit is further configured to present said

data signals in a first predetermined pattern such that said second frequency is an integer fraction of said first frequency.

4. (ORIGINAL) The prescaler according to claim 3, wherein said second circuit is further configured to present said data signals in a second predetermined pattern such that said second frequency equals said first frequency.

5. (CURRENTLY AMENDED) The prescaler according to claim 1, further comprising a plurality of latches configured to latch said data signals presented by said second circuit, wherein said second circuit presents said data signals directly to said latches instead of said multiplexer.

6. (ORIGINAL) The prescaler according to claim 5, wherein said latches are further configured to sample said data signals in a staggered order in response to said control signals.

7. (ORIGINAL) The prescaler according to claim 1, wherein said first circuit is further configured to present one of said control signals in an active state at a time.

8. (ORIGINAL) The prescaler according to claim 1, wherein said first circuit is further configured to present at least two of said control signals in an active state at a time.

9. (CURRENTLY AMENDED) The prescaler according to claim 1, further comprising:

a first dividing circuit configured to divide said second clock signal by a first predetermined integer to present a third clock signal; and

a second dividing circuit configured to divide said third clock signal by a second predetermined integer to present a fourth clock signal; and

~~a gating circuit configured to gate said second clock signal received by said second circuit in response to said third clock signal and said fourth clock signal.~~

10. (CURRENTLY AMENDED) The prescaler according to claim 9, further comprising a circuit configured to control said fourth clock signal ~~to select a modulus of division of said first clock signal.~~

11. (CURRENTLY AMENDED) A method of dividing a first clock signal having a first frequency, the method comprising the steps of:

(A) generating a plurality of control signals in response to said first clock signal;

(B) multiplexing a plurality of data signals in response to said control signals to present a second clock signal having a second frequency that is a non-integer fraction of said first frequency; and

10 (C) generating said data signals in response to said
second clock signal; and

(D) presenting said data signals directly to said multiplexing.

12. (ORIGINAL) The method according to claim 11, further comprising the step of sequencing said data signals through a plurality of patterns response to said second clock signal.

13. (ORIGINAL) The method according to claim 11, further comprising the step of presenting said data signals to said multiplexing in a first predetermined pattern such that said second frequency is an integer fraction of said first frequency.

14. (ORIGINAL) The method according to claim 13, further comprising the step of presenting said data signals to said multiplexing in a second predetermined pattern such that said second frequency equals said first frequency.

15. (CURRENTLY AMENDED) The method according to claim 11, further comprising the step of latching said data signals in response to generating said data signals, wherein step (D) presents said data signals directly to said latching instead of said multiplexing.

16. (ORIGINAL) The method according to claim 15, wherein the step of latching further comprises the sub-step of sampling said data signals in a staggered order in response to said control signals prior to multiplexing.

17. (ORIGINAL) The method according to claim 11, wherein the step of generating said plurality of control signals comprises the sub-step of presenting one of said control signals in an active state at a time.

18. (ORIGINAL) The method according to claim 11, wherein the step of generating said plurality of control signals comprises the sub-step of presenting at least two of said control signals in an active state at a time.

19. (ORIGINAL) The method according to claim 11, further comprising the steps of:

dividing said second clock signal by a first predetermined integer to present a third clock signal;

5 dividing said third clock signal by a second predetermined integer to present a fourth clock signal; and

gating said second clock signal in response to said third clock signal and said fourth clock signal prior to generating said data signals.

20. (CURRENTLY AMENDED) A prescaler comprising:

means for generating a plurality of control signals in response to said a first clock signal;

5 means for multiplexing a plurality of data signals in response to said control signals to present a second clock signal having a second frequency that is a non-integer fraction of said first frequency; and.

means for generating said data signals in response to said second clock signal.

21. (NEW) A prescaler comprising:

a first circuit configured to generate a plurality of control signals in response to a first clock signal having a first frequency;

5 a multiplexer configured to multiplex a plurality of data signals in response to said control signals to present a second

clock signal having a second frequency that is a non-integer fraction of said first frequency;

10 a second circuit configured to generate said data signals
in response to said second clock signal;

a first dividing circuit configured to divide said second clock signal by a first predetermined integer to present a third clock signal;

15 a second dividing circuit configured to divide said third
clock signal by a second predetermined integer to present a fourth
clock signal;

a gating circuit configured to gate said second clock signal received by said second circuit in response to said third clock signal and said fourth clock signal; and

20 a circuit configured to control said fourth clock signal
to select a modulus of division of said first clock signal.

22. (NEW) The prescaler according to claim 9, further comprising:

a gating circuit configured to gate said second clock signal received by said second circuit in response to said third 5 clock signal and said fourth clock signal.

23. (NEW) The method according to claim 19, further comprising the step of:

controlling said fourth clock signal to select a modulus of division of said first clock signal.